High Linearity CMOS SOI Mixer

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Abstract — This paper describes the design of a single-ended CMOS SOI mixer with very high linearity. The mixer delivers +23dBm of IIP3 with a conversion loss of 6.5dB at an RF frequency of 1.9GHz, at an LO drive of 0dBm and a bias current of 6.3mA at $3V_{DC}$. The mixer is fabricated in a 0.5μm CMOS SOI process and operates over a frequency range of 900MHz to 2.4GHz drawing 6-8mA of supply current (dependant on LO drive) at a DC supply of only 3V. The chip size is 466μm x 606μm and is housed in a six lead SOT-23 package.

I. Introduction

Mixers are required in communications circuits to provide the frequency translation from baseband signals to radio frequencies and vice versa. Some important linearity characteristics of mixers are the "1dB Compress Point" and the "3rd Order Intercept Point" which are measures of the unwanted distortion characteristics inherent in these circuits [1]. Linearity is strongly dependant on the characteristics of the active devices and often requires unacceptably high power to achieve the specifications required for many of today's high performance communications standards such as IS95 (Code Division Multiple Access). This design incorporates an LO buffer, which allows for a lower drive level while maintaining exceptional linearity performance. It's single ended nature eliminates the need for large, costly baluns often necessary in differential type mixers.

II. Process Description

The mixer was fabricated with the Peregrine UTSi 0.5mm process. Fig. 1 summarizes the differences between UTSi and bulk CMOS process. UTSi is a thin silicon layer deposited on a synthetic sapphire wafer, which allows the use of standard silicon fabrication equipment and processing techniques. High levels of integration and the capability of realizing partially and fully depleted devices, as well as near ideal passives are a few advantages of this process. Also, deep isolation wells present in the bulk CMOS process are unnecessary, simplifying the UTSi transistor processing and increasing circuit density [2].

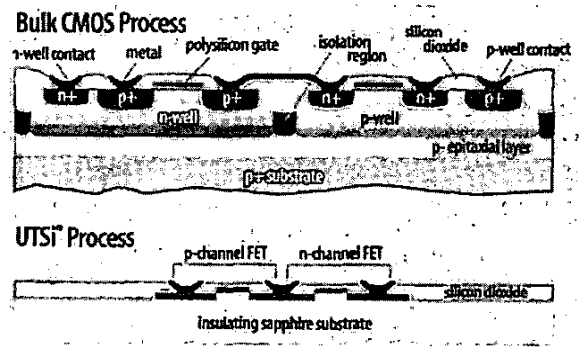

Fig. 1. Cross section diagram contrasting the differences between the SOI and typical bulk CMOS processes

III. Mixer Circuit Background

The mixer is comprised of a local oscillator (LO) input with a buffer amplifier which drives the mixer switching device. The radio frequency (RF) and intermediate frequency (IF) pins are interchangeable. Three additional pins for DC bias (one V_{DD} pin, two GND pins) are used.

Fig. 2 shows the typical application circuit for this mixer. The basic operation of the mixer can best be described by observing Fig. 3.

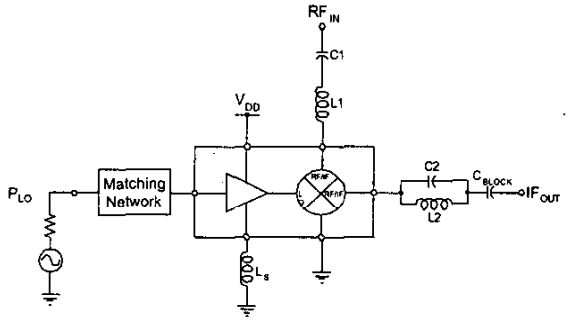

Fig. 2. Mixer application circuit

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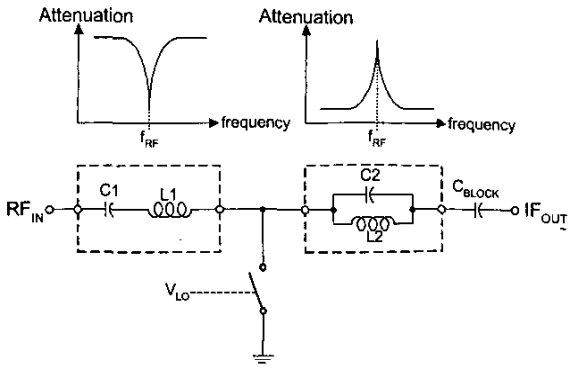

Fig. 3. Diagram of the fundamental operation of the mixer

The mixer uses external resonant components to select the RF and IF signals. A series resonant circuit (L1 and C1) passes only the RF frequency to the first terminal of the switch and rejects the IF and LO frequencies at the RF_{IN} port. A parallel resonant circuit (L2 and C2) rejects the RF signal present at the first terminal of the switch and passes the IF signal to the IF_{OUT} port. The frequency translation of the RF input to the IF output is accomplished by the opening and closing of the switch at the LO frequency rate. This ideal mixer can achieve a maximum conversion gain of -3.9dB.

IV. Mixer Circuit Design

The mixer design deviates from the ideal due to the effects of:

- ON and OFF series resistance
- Series inductance
- Parasitic capacitance
- Non-symmetric LO switching
- Drive voltage required for LO switching

The ideal switch will be realized by a MOSFET device that has been selected based on the design criteria developed in the following sections.

A. On and Off Series Resistance

If the switch has a finite ON and OFF resistance (R_{ON} and R_{OFF}), the conversion gain is given by (1).

$$G = \frac{2}{\pi}\left[\frac{R_{OFF}R_S - R_S R_{ON}}{(R_S + R_{OFF})(R_S + R_{ON})}\right] \quad (1)$$

Equation (1) shows that in order to obtain -6dB of conversion gain, the following series resistance values are required:

$$R_{ON} \le 13.7\Omega$$
$$R_{OFF} \ge 183\Omega \quad (2)$$

B. Series Inductance

In addition to the series resistance, the series inductance of the package must be considered. Series inductance has the same effect on the conversion gain as the series ON resistance (R_{ON}). The maximum R_{ON} is now modified by (3) where L_S and L_D are the series source and drain inductances respectively.

$$|Z_{ON}| = \sqrt{R_{DS(ON)}^2 + \omega^2(L_S + L_D)^2} \quad (3)$$

Using the previous derivation for a conversion gain of –6dB and assuming L_S=L_D=1nH and ω_{RF}=1GHz requires that $R_{DS(ON)} \le 5.36\Omega$.

C. Parasitic Capacitance

The parasitic capacitance of the switching FET effectively lowers the OFF resistance. Fig. 4 shows a plot of the effect of C_{GD} on the series OFF resistance versus operating frequency. A large switch device with low R_{ON} is feasible due to the decreased parasitic capacitance in the UTSi process, maintaining a sufficiently high R_{OFF}.

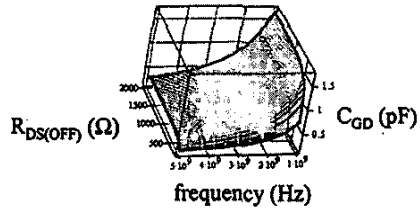

Fig. 4. OFF impedance as a function of C_{GD} and operating frequency

D. Non-symmetric LO Switching

In addition to effects of the finite switch resistance, the duty cycle of the LO signal has an impact on the conversion gain of the mixer as given by (4) (where σ is the LO duty cycle). The LO duty cycle is affected by the buffer amplifier and its ability to symmetrically drive the mixer switching device.

$$G = \frac{2|\mathrm{sinc}(\pi\sigma)|}{|V_{RF}|} \quad (4)$$

E. Device Requirements

These constraints are then utilized to select an appropriate device for the mixer switch. The switching FET will operate in the triode region since no DC bias will be con-

nected to the device drain ($V_{DS(DC)}$=0V). Equation (5) describes the MOSFET series resistance in the triode region [3]. This equation is used to determine the device size required to satisfy (2) and (3).

$$R \approx \frac{1}{\mu C_{OX}\frac{W}{L}(V_{GS}-V_T)} \quad (5)$$

Lowest $R_{DS(ON)}$ requires:

- High μC_{OX}
- Large W/L
- High gate drive voltage, such that $V_{GS}>>V_T$

The series resistance of the device is also a function of V_{GS} and the device threshold voltage (V_T) as shown in (5). Fig. 5 shows a plot of the static resistance characteristics of three devices with the same area but different threshold voltages (standard, low and zero V_T).

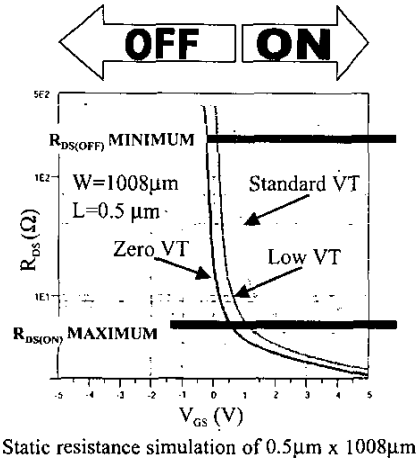

Fig. 5. Static resistance simulation of 0.5µm x 1008µm NMOS devices

From the static device simulations, a Low V_T type device was selected for use as the mixer switch. The Low V_T device was selected over the Zero V_T device, which has a lower ON resistance, because the Low V_T device did not require as much negative gate voltage drive to achieve the maximum $R_{DS(OFF)}$.

The gate of the switching device must be driven with a voltage such that the device will be driven into a minimum resistance for the ON state and a maximum resistance for the OFF state. Therefore it is necessary to use an inductor to resonate the LO buffer output so as to provide maximum voltage swing to the gate of the switching device. Also, from Fig. 5 it can be seen that to insure maximum resistance, the device must be driven with a sufficiently negative voltage. Due to the need for a negative gate drive voltage, the LO buffer was realized with a PMOS device and a bias inductor connected to ground as shown in Fig. 6.

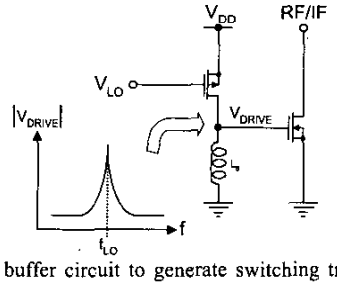

Fig. 6. LO buffer circuit to generate switching transistor gate drive

Since a large negative swing is possible on the gate of the switching device, a clamp circuit is employed to insure that the negative voltage does not exceed the device breakdown level.

Finally, the LO buffer device requires a bias circuit. A simple current mirror bias is employed which allows the user to control the LO buffer bias by means of an external resistor.

F. Packaging

Based on the design information, a package with minimum series inductance is required to realize the lowest series inductance. A six lead SOT-23 package with body dimensions of 5mm x 1.6mm was used. This package has a lead and bond wire inductance of approximately 1nH.

G. Die

Fig. 7 shows a photograph of the mixer die. The die size is 466µm x 606µm.

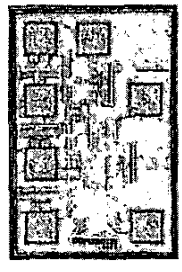

Fig. 7. Photograph of the mixer die

V. Results

Mixer evaluation results for RF frequencies of 1100MHz (Fig. 8 and Fig. 9) and 1950MHz (Fig. 10 and Fig. 11) are presented. These plots include conversion loss and third order intercept point vs. RF frequency and LO power. The RF and IF external resonant circuits were modified for opti-

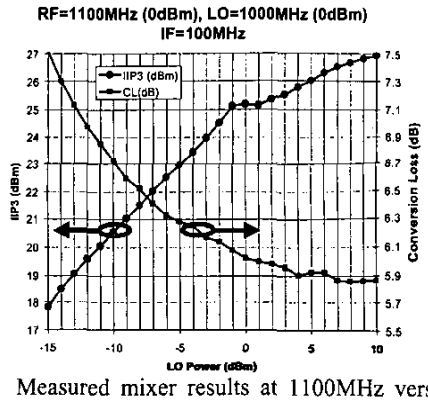

Fig. 8. Measured mixer results at 1100MHz versus LO drive power

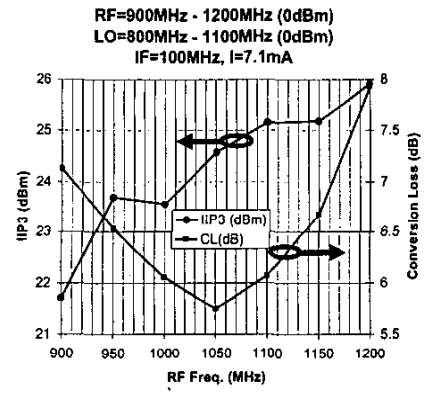

Fig. 9. Measured mixer results at a fixed LO drive power of 0dBm versus frequency centered at 1100MHz

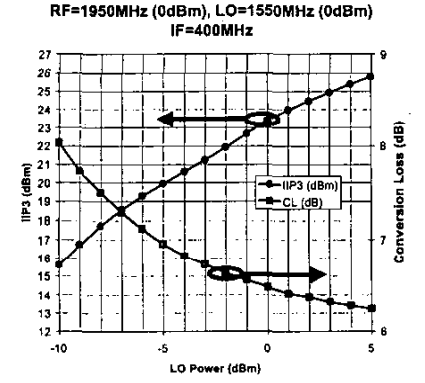

Fig. 10. Measured mixer results at 1950MHz versus LO drive power

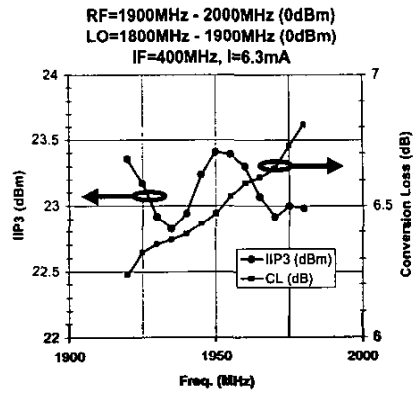

Fig. 11. Measured mixer results at a fixed LO drive power of 0dBm versus frequency centered at 1950MHz

VI. Conclusions

This paper describes the design of a high linearity CMOS SOI mixer that operates over a wide frequency range and with minimal LO and DC power. The mixer is designed so as to address a wide range of both portable and stationary wireless and wired applications requiring low distortion and low power gain. In addition, the device is capable of bias control allowing an additional degree of freedom in its use.

VII. References

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